Family 10h
AMD Phenom™ Processor
Product Data Sheet

Publication # 44109
Revision: 3.00
Issue Date: November 2007

Revision History

Date	Revision	Description
November 2007	3.00	Initial Public Release

1 Family 10h AMD Phenom™ Processor Features

The following is a list of features and capabilities of the Family 10h AMD Phenom™ processor.

- **Compatible with Existing 32-Bit Code Base**
  - Including support for SSE, SSE2, SSE3, SSE4a, ABM, MMX™, 3DNow!™ technology and legacy x86 instructions
  - Runs existing operating systems and drivers
  - Local APIC on the chip
- **AMD64 Technology**
  - AMD64 technology instruction set extensions
  - 64-bit integer registers, 48-bit virtual addresses, 40-bit physical addresses
  - Sixteen 64-bit integer registers
  - Sixteen 128-bit SSE/SSE2/SSE3 registers
- **Multi-Core Architecture**
  - Triple-core or quad-core options
  - AMD Balanced Smart Cache
    - Discrete L1 and L2 cache structures for each core
    - Shared L3 cache structure
- **Machine Check Architecture**
  - Includes hardware scrubbing of major ECC protected arrays
- **Cache Structures**
  - **64-Kbyte 2-Way Associative ECC-Protected L1 Data Cache**
    - Two 64-bit operations per cycle, 3-cycle latency
  - **64-Kbyte 2-Way Associative Parity-Protected L1 Instruction Cache**
    - With advanced branch prediction
  - **512-Kbyte 16-Way Associative ECC-Protected L2 Cache**
    - Exclusive cache architecture storage in addition to L1 caches
  - **2048-Kbyte (2-Mbyte) Maximum 32-way Associative ECC-Protected L3 Cache**
    - Shared cache architecture storage in addition to exclusive L1 and L2 caches
- **Floating-Point Unit**
  - AMD Wide Floating-Point Accelerator
    - 128 bit Floating-Point Unit (FPU)
- **Virtualization Features**
  - SVM disable and lock
  - Nested paging
  - Rapid Virtualization Indexing
- **Power Management**
  - Multiple low-power states
  - Independent Dynamic Core Technology
  - AMD CoolCore™ Technology
  - Dual Dynamic Power Management
  - System Management Mode (SMM)
  - ACPI-compliant, including support for processor performance states
  - Supported power states: C0, C1, C1E, S0, S1, S3, S4, S5
- **Electrical Interfaces**
  - DDR2 SDRAM: SSTL_1.8 per JEDEC specification
  - DDR2 SDRAM-like electrical specifications also used for clock, reset and test signals

  - Refer to the *AMD Family 10h Processor Electrical Data Sheet, order# 40014*, for electrical details of AMD Family 10h processors.
- **HyperTransport™ Technology to I/O Devices**
  - HyperTransport 1 and HyperTransport 3 technology supported
  - One (1) link, 16-bits in each direction, supporting up to 2000 MT/s or 4.0 GB/s in each direction in HyperTransport Generation 1.0 mode and 3600 MT/s or 7.2 GB/s in each direction in HyperTransport Generation 3.0 mode.
- **Integrated Memory Controller**
  - AMD Memory Optimizer Technology
  - Low-latency, high-bandwidth
  - ECC checking with double-bit detect and single-bit correct
  - 144-bit DDR2 SDRAM controller operating at frequencies up to 533 MHz
  - Supports up to four unbuffered DIMMs
- **Available Packages**
  - Compliant with RoHS (EU Directive 2002/95/EC) with lead used only in small amounts in specifically exempted applications
  - Package AM2r2
    - Refer to the *AM2r2 Processor Functional Data Sheet, order# 41697*, for functional and mechanical details of the AM2r2 package processor.
    - 940-pin lidded micro PGA
    - 1.27-mm pin pitch
    - 31 x 31 row pin array
    - Organic C4 die attach

2 Compatible Socket Infrastructures

Refer to the *AMD Infrastructure Roadmap, order# 41842* for information on platform feature implications of package and socket infrastructure combinations. Family 10h AMD Phenom™ processors support the following socket infrastrucutres:

- **Socket AM2 Socket Infrastructure**
  - Compatible with AM2 and AM2r2 package processors
  - Refer to the *Socket AM2 Processor Functional Data Sheet, order# 31117*, for functional and mechanical details of the AM2 socket**.**
- **Socket AM2r2 Socket Infrastructure**
  - Compatible with AM2 and AM2r2 package processors
  - Refer to the *AM2r2 Processor Functional Data Sheet, order# 41697*, for functional and mechanical details of the AM2r2 socket**.**